NU8500Q

64 Pin, 16-Bit Digital Signal Controllers with High-Resolution PWM and CAN Flexible Data (CAN FD)

Operating Conditions

- 3.0V to 3.6V, -40°C to +125°C, DC to 100 MIPS

Core: 16-Bit CPU

- 256 Kbytes of Program Flash with ECC and 24K RAM
- Fast 6-Cycle Divide
- Live Update
- Code Efficient (C and Assembly) Architecture
- 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL Plus Hardware Divide
- 32-Bit Multiply Support
- Four Sets of Interrupt Context Saving Registers which Include Accumulator and STATUS for Fast Interrupt Handling
- Zero Overhead Looping
- RAM Memory Built-In Self-Test (MBIST)

Clock Management

- Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Reference Clock Output
- Fail-Safe Clock Monitor (FSCM)
- Fast Wake-up and Start-up
- Backup Internal Oscillator

Power Management

- Low-Power Management Modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset

High-Speed PWM

- 8 PWM Pairs
- Up to 250 ps PWM Resolution
- Dead Time for Rising and Falling Edges
- Dead-Time Compensation
- Clock Chopping for High-Frequency Operation
- Fault and Current Limit Inputs
- Flexible Trigger Configuration for ADC Triggering

Timers/Output Compare/Input Capture

- One General Purpose Timer
- Peripheral Trigger Generator (PTG):
  - Up to 15 trigger sources to other peripheral modules
  - CPU independent state machine-based instruction sequencer
- Nine MCCP/SCCP modules which Include Timer, Capture/Compare and PWM:
  - 1 MCCP
  - 8 SCCPs
  - 16 or 32-bit time base
  - 16 or 32-bit capture
  - 4-deep capture buffer
- Fully Asynchronous Operation, Available in Sleep Modes

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Advanced Analog Features

- High-Speed ADC module:
  - 12-bit with two dedicated SAR ADC cores and one shared SAR ADC core
  - Configurable resolution (up to 12-bit) for each ADC core
  - Up to 3.5 Msps conversion rate per channel at 12-bit resolution
  - Up to 20 input channels
  - Dedicated result buffer for each analog channel
  - Flexible and independent ADC trigger sources
  - Four digital comparators
  - Four oversampling filters for increased resolution
- Up to Three Analog Comparators:
  - 15 ns analog comparator
- Up to Three Op Amps
- One 12-Bit DAC:
  - Hardware slope compensation

Communication Interfaces

- Three Protocol UARTs with Automated Protocol Handling Support for:
  - LIN 2.2
  - DMX
  - IrDA®
- Three 4-Wire SPI/I^2S modules
- CAN Flexible Data (FD) module
- Three I^2C modules with SMBus Support
- PPS to Allow Function Remap
- Programmable Cyclic Redundancy Check (CRC)
- Two SENT modules
- Parallel Master Port (PMP)

Direct Memory Access (DMA)

- Four DMA Channels

Debugger Development Support

- In-Circuit and In-Application Programming and Debugging
- Three Complex, Five Simple Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace Buffer and Run-Time Watch

Safety Features

- Clock Monitor System with Backup Oscillator
- DMT (Deadman Timer)
- ECC (Error Correcting Code)
- WDT (Watchdog Timer)
- CodeGuard™ Security
- CRC (Cyclic Redundancy Check)
- Flash OTP by ICSP™ Write Inhibit
- RAM Memory Built-In Self-Test (MBIST)
- Two-Speed Start-up
- Fail-Safe Clock Monitoring (FSCM)
- Backup FRC (BFRC)
- Capless Internal Voltage Regulator
- Virtual Pins for Redundancy and Monitoring

Functional Safety

- Class B Safety Library – IEC 60730
- For ASIL B and Beyond Applications – ISO 26262
- FMEDA Computation Spreadsheet (Evaluation of Random Hardware Failures Metric)
- Functional Safety Manual
- Functional Safety Diagnostics Suite

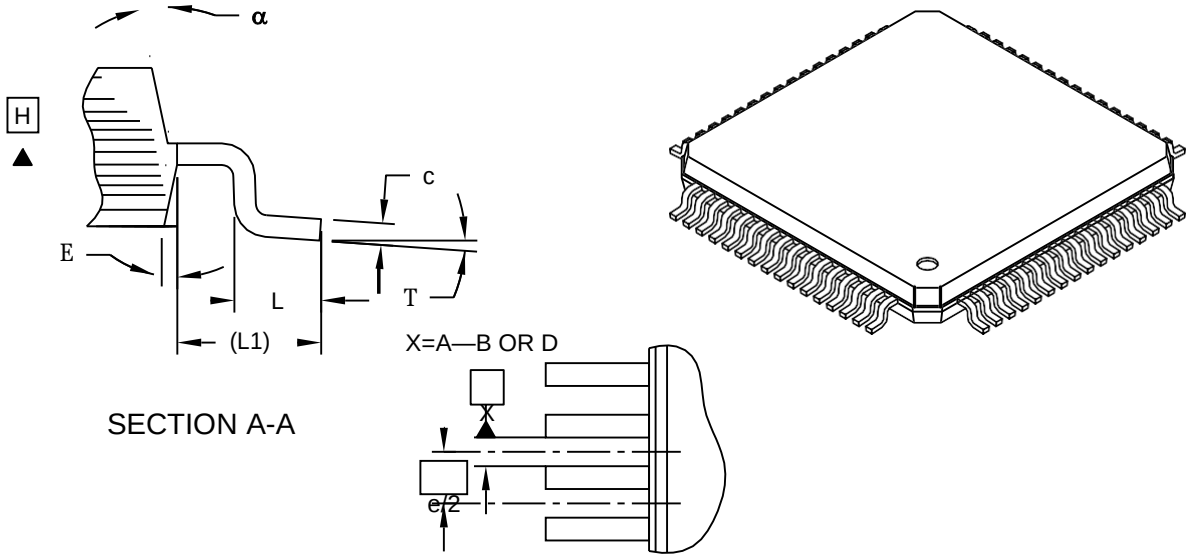
Qualification Support

- AEC-Q100 REV-H (Grade 1: -40°C to +125°C) Compliant

27.0 PACKAGING INFORMATION

27.1 Package Details

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]



SECTION A-A

DETAIL 1

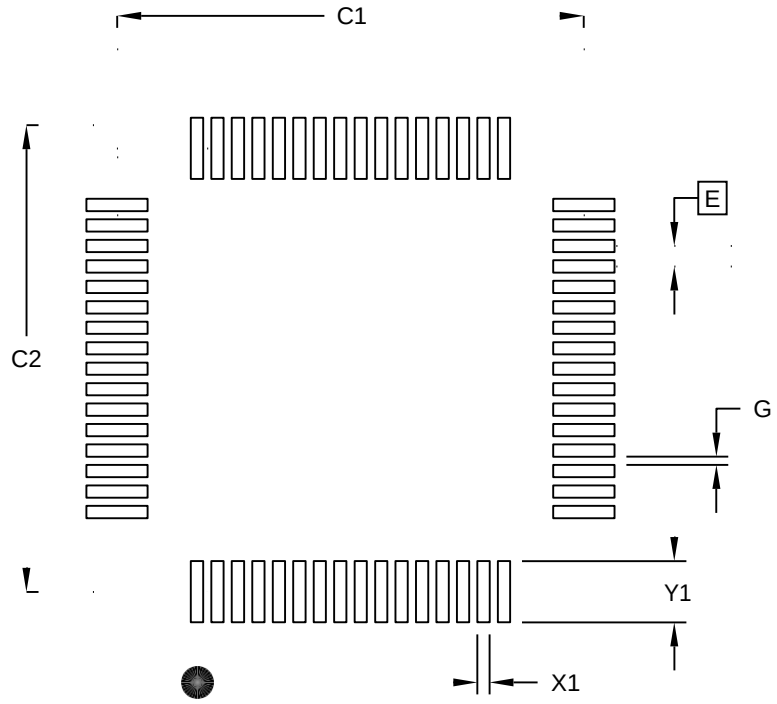
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	I	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	D	11°	12°	13°
Mold Draft Angle Bottom	E	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

64- Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerance