# AN2000 APPLICATION NOTE

（AN2000 应用手册）

# NU2105-based Charge Pump 2:1&1:1 Design

（设计手册）

## 1 Introduction（简介）

- 97.5% Efficient at 2:1 charge mode, 99.2% Efficient at 1:1 charge mode Power Stage for 8-A Fast Charge
- 8 Channel Hardware Protections and 7channel Software alarms.
- Low ON-Resistance of power MOSFET with high efficiency
- The maximum frequency reach to 1MHz to be possible reducing the FLYCAP capacitance
- Package with 56-WCSP 2.8mm x 3.2mm, 0.4mm pitch

## 2 Applications（应用）

- Smart Phone
- Table PC



# 3 Typical Design

Typical schematic of Standalone and Parallel operation,

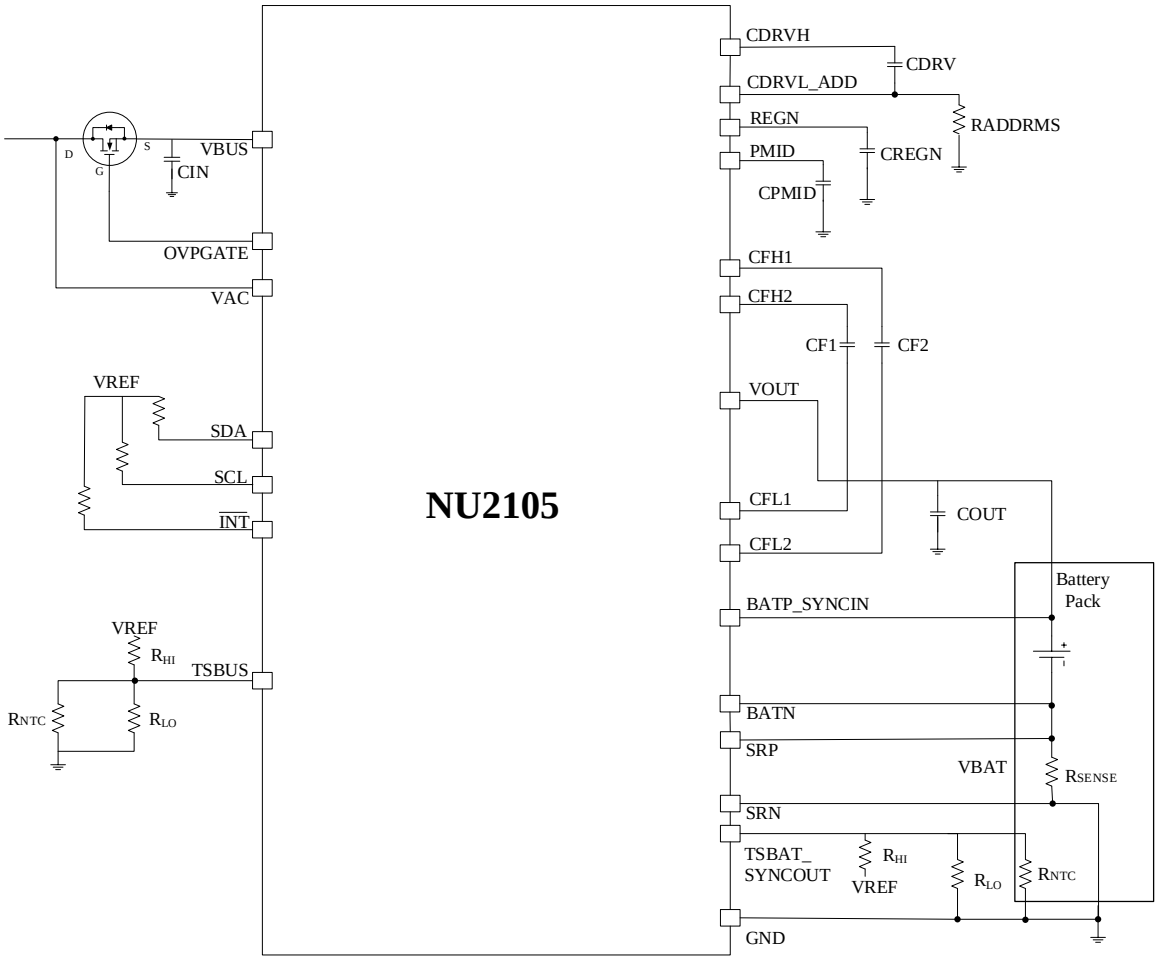



**Figure 1. Typical Schematic - Standalone**

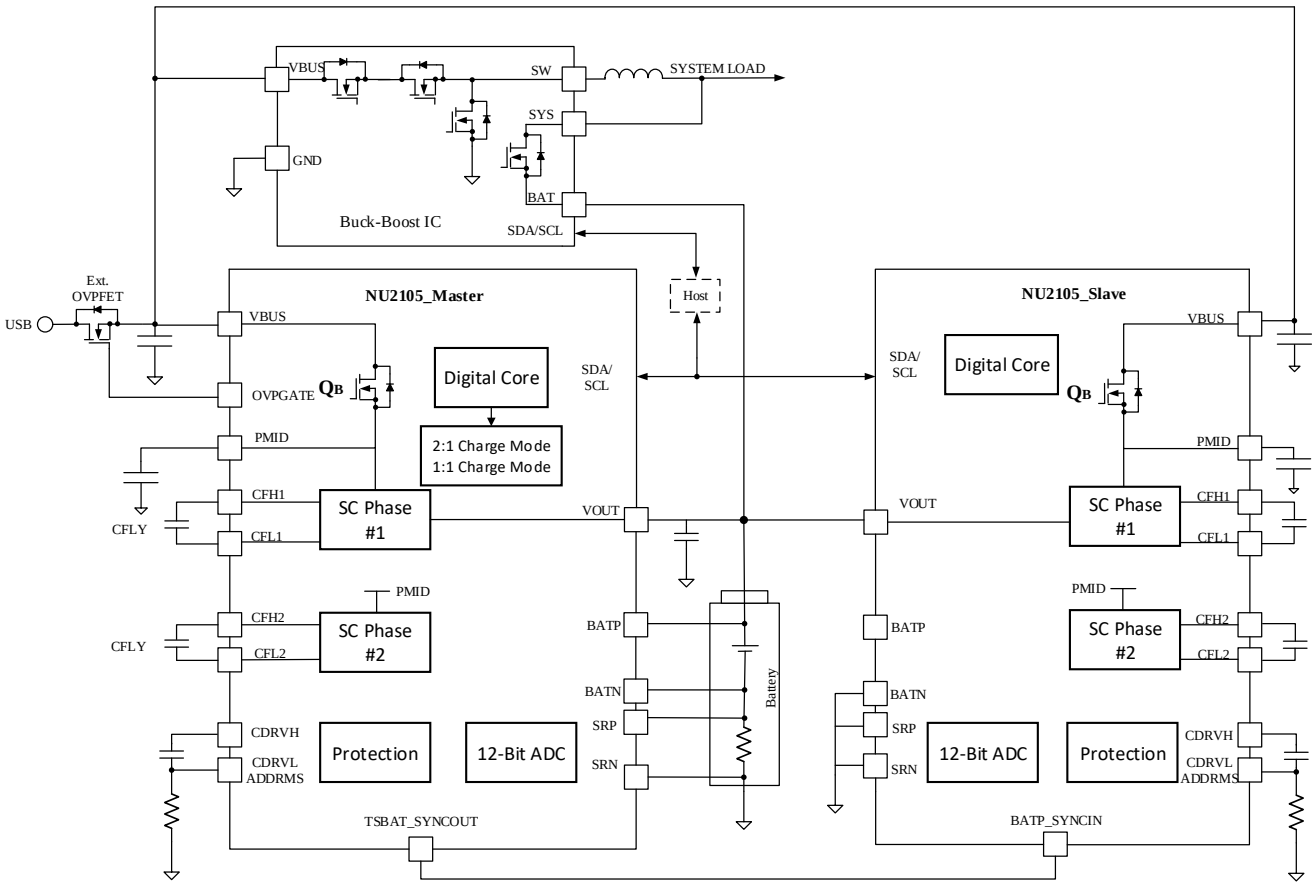



**Figure 2. Typical Schematic - Parallel**

# 4 2:1 and 1:1 Charging Profile

Figure 3 is the equivalent system charging structure of charging pump.

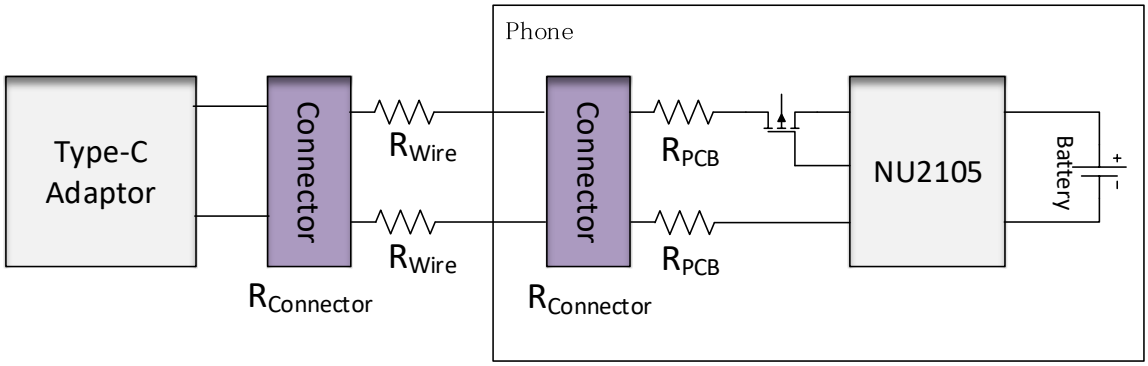



**Figure 3. Equivalent System Charging Structure**

From the point of view of minimizing the power loss within phone, consider the phone efficiency of all components in the phone loop, which include the internal Connector $R_{Connector}$, PCB impedance

$R_{PCB}$, $R_{NMOS}$ and loss on NU2105. Figure 4 shows the phone efficiency Calculation with 2:1 and 1:1 charging mode.

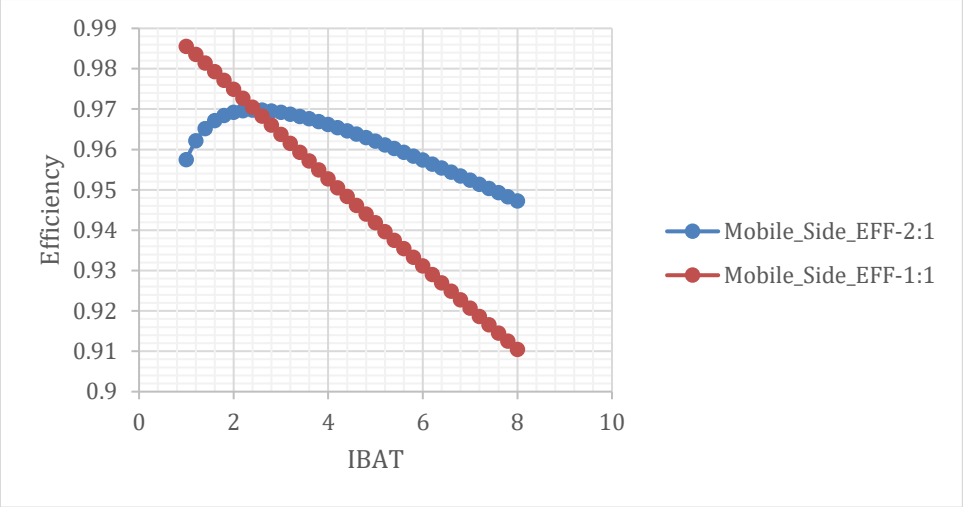



**Figure 4. Phone Efficiency with 2:1 and 1:1 Charging Mode**

To get the maximum of phone efficiency, use 1:1 charging mode at low-side charging current (for example <3A) and convert to 2:1 charging mode at high-side charging current (for example >=3A).

Figure 5 shows the IC itself efficiency at 2:1 and 1:1 charging mode @500KHz.

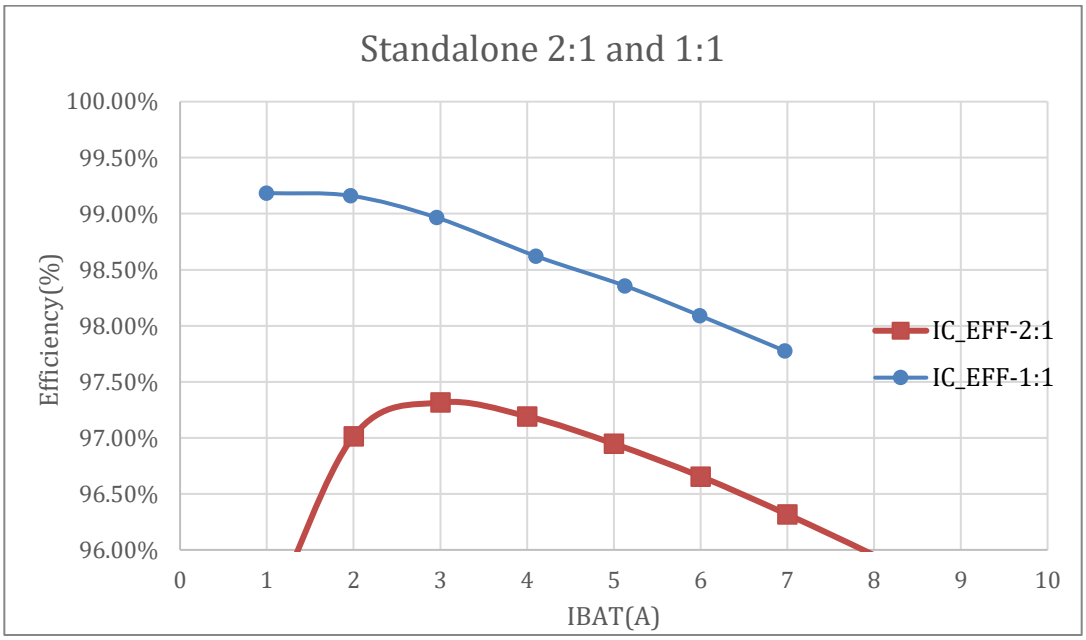



**Figure 5: IC Efficiency with 2:1 and 1:1 Charging Mode**

# 5 GUI Tool Introduction

The GUI is developed based on the OnEasy USB to I²C driver.

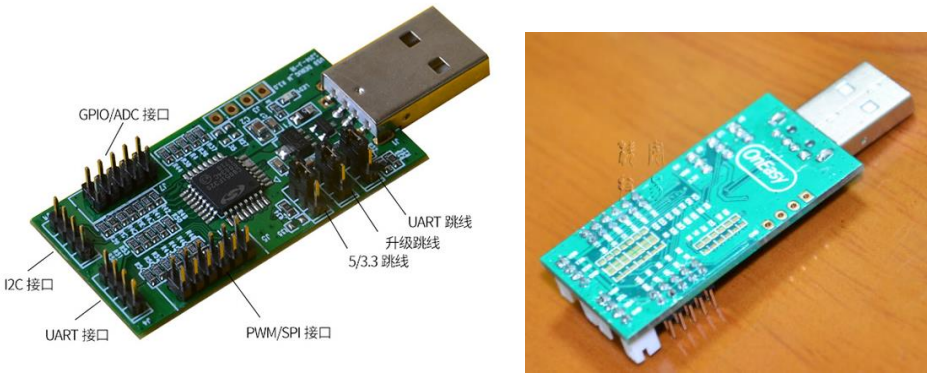
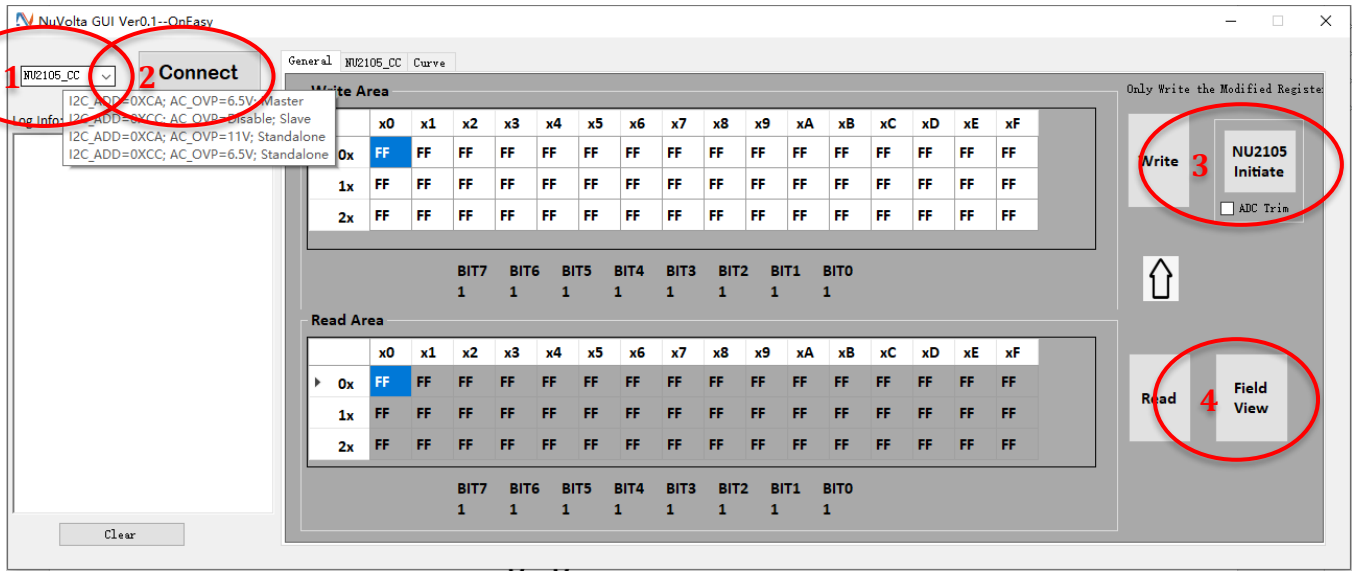


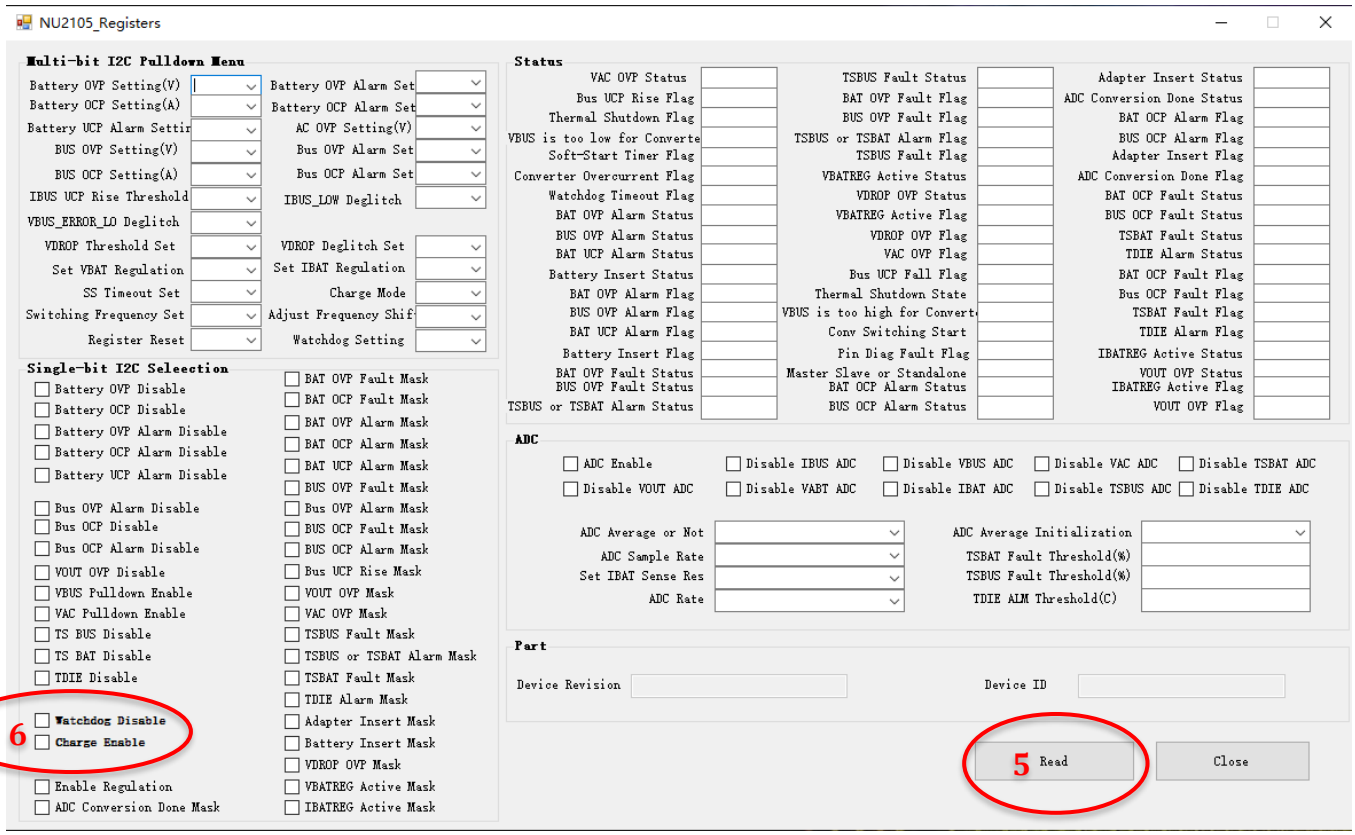

**Figure 6: OnEasy Driver**

1. Select the appreciate part from drop-down text. There are two I²C address according to the configuration on CDRVL_ADDRMS pin.

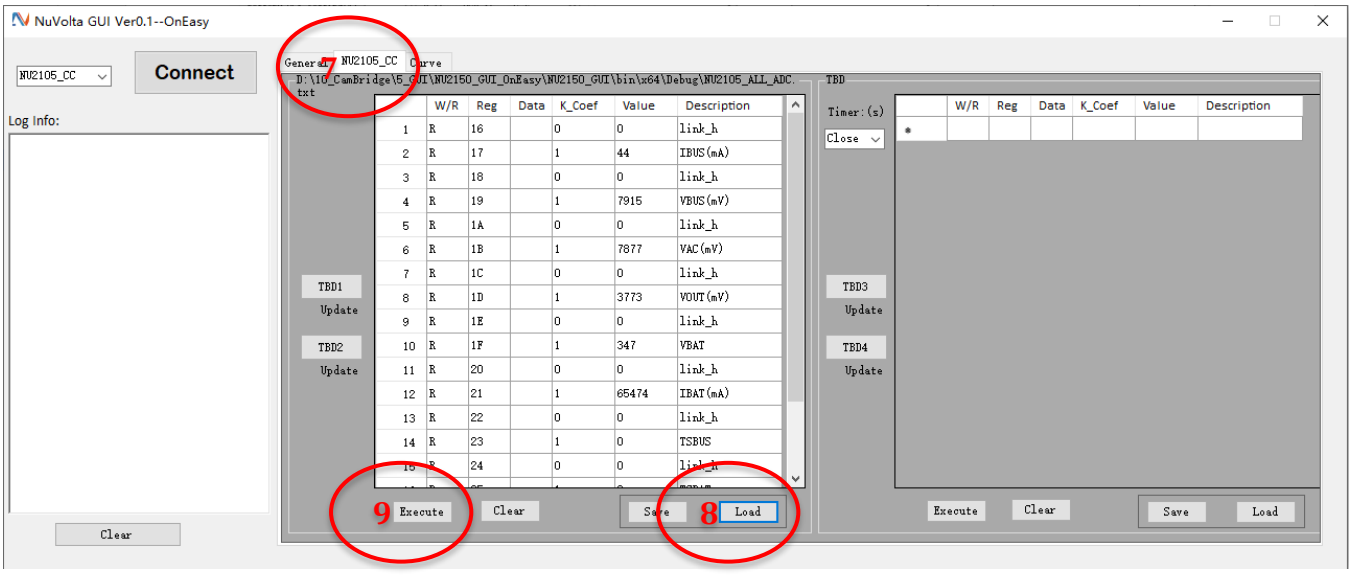
| | | | | |
|---|---|---|---|---|
| NU2105_CA | I2C_Address=0x65 | AC_OVP=6.5V | Master | 18kΩ |
| NU2105_CC | I2C_Address=0x66 | AC_OVP disable | Slave | 39kΩ |
| NU2105_CA | I2C_Address=0x65 | AC_OVP=11V | Standalone | 75kΩ |
| NU2105_CC | I2C_Address=0x66 | AC_OVP=6.5V | Standalone | Open (>150kΩ) |




2. Click ‘Connect’ button.
3. Click ‘NU2105 Initiate’ button to initiate some default value to related registers.
4. Click ‘Field View’ open another form.
5. Click ‘Read’ button to see all the register status.
6. Click ‘Charge Enable’ to start charge.




7. Click 'NU2105_Cx' to open another tab which provide the function to read or write any registers. 'K_Coef' is the multiplier of 'Data', the result is showed at 'Value'.
8. Or Click 'Load' to load the existing register operation file.
9. Click 'Execute' to execute the action items showed in the above grid.



# 6 Notification of 1:1 Charging Mode

At 1:1 charging mode, the threshold of VBUS_OVP is the half of the value set in the register of 0x06h. The range is 3V to 6.17V, step is 25mV.
And the VAC_OVP is fixed with 5.5V at this mode.
At this mode, the VBUS_OVP_ALM will be disabled, since the voltage drop on VBUS and VBAT is very small, VBUS_OVP_ALM can be replaced by VBAT_OVP_ALM at application.

# 7 ADC and Efficiency Measurement

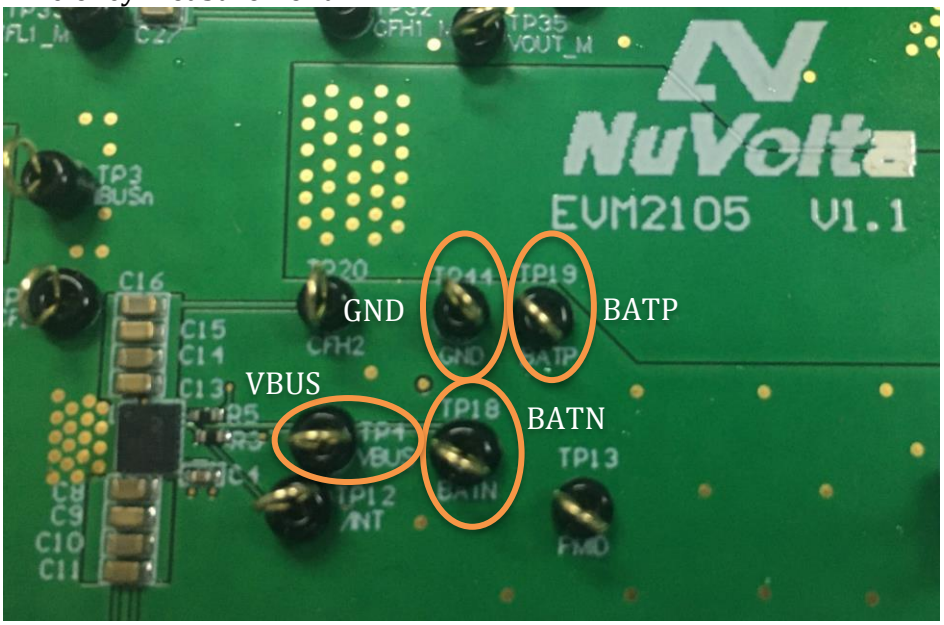
Voltage ADC Measurement:

1. VAC, TP7 (VAC) to TP44 (GND)
2. VBUS, TP4 (VBUS) to TP44 (GND)
3. VOUT, TP19 (BATP) to TP44 (GND)
4. VBAT, TP19 (BATP) to TP18 (BATN)

Current ADC Measurement:

1. IBAT, read from J2 wire
2. IBUS, IBAT/2 or read from J1 wire minus the quiescent current from IC.

Efficiency Measurement:




1. IIN=IAC (read from J1 wire) - $I_{Others}$ (the current dissipated by other components)
2. P_BAT=VOUT*IBAT (BATP, GND)
3. P_BUS=VBUS*IIN (VBUS, GND)
4. IC_Efficiency=P_BAT/P_BUS

Temperature ADC Measurement:

1. TSBAT, TP16 (TSBAT_S) to TP45 (AGND)
2. TSBUS, TP88 (TSBUS) to TP45 (AGND)

3. TSBUS Master, TP26 (TSBUS_M) to TP45 (AGND)

# 8 Layout Guideline

Layout is very important to maximize the electrical and thermal performance of the total system. General guidelines are provided, but the form factor, board stack-up, and proximity of the other components also need to be considered to maximize the performance.

- VBUS traces should be as short and wide as possible to accommodate for high current.
- Minimize losses through connectors wherever possible, as the losses in these connectors will contribute a significant amount to the total power loss.
- Use visa under the exposed thermal pad for thermal relief.
- Place low ESR bypass capacitors to ground for VBUS, PMID, and VOUT. The capacitor should be placed as close to the device pins as possible.
- The CFLY pads should be as small as possible, and the CFLY caps placed as close as possible to the device, as these are switching pins and this will help reduce EMI.
- Connect all quiet signals to the AGND pin(s).
- Connect all power signals to the PGND pin(s).

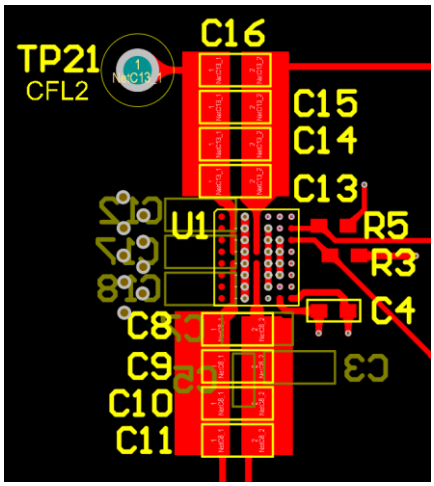



**Figure 7. NU2105 Layout Example – Top Layer**

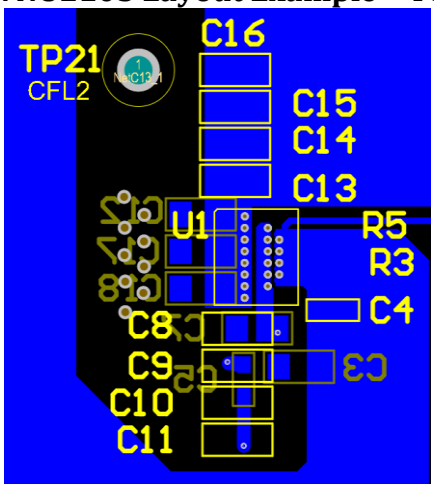


**Figure 8. NU2105 Layout Example – Bottom Layer**

# 9 Revision Histories

| | Date | Changes |
|---|---|---|
| V1.0 | May/29/2020 | Draft version. |
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